READ-WHILE-WRITE FLASH MEMORY DEVICES HAVING LOCAL ROW DECODER CIRCUITS ACTIVATED BY SEPARATE READ AND WRITE SIGNALS

ABSTRACT

A flash memory device can include a local row decoder circuit that is configured to drive word lines coupled to a bank of a flash memory responsive to separate read and write control signals provided thereto from outside the local row decoder circuit. Multiple local row decoder circuits can, therefore, be controlled by a single global row decoder circuit that provides the separate read and write control signals to each of the local row decoder circuits. By locating the combinatorial logic circuits used for decoding addresses in the global row decoder circuit, rather than in the local row decoder circuits, the local row decoder circuits may have reduced size, thereby allowing further reductions in the size of the flash memory device. For example, in some embodiments according to the invention, a NAND logic circuit used for address decoding is located in the global row decoder circuit, thereby allowing the area allocated to the local row decoder circuit to be reduced. Furthermore, because the may be many local row decoder circuits implemented in the flash memory device, the total size of the flash memory may be reduced.